(10) ABSTRACT

Wafer-level chip-scale packaging technology is used for improving performance or reducing size of integrated circuits by using metallization of pad-to-bump-out beams as part of the integrated circuit structure. Chip-scale packaging under bump metal is routed to increase the thickness of top metal of the integrated circuit, increasing current carrying capability and reducing resistance. An exemplary embodiment for a power MOSFET array integrated structure is described. Another exemplary embodiment illustrated the use of chip-scale processes for interconnecting discrete integrated circuits.